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ABSTRACT OF THE DISCLOSURE

A method for synthesizing a registered transfer level (RTL) based design employs a bottom-up approach to generate a final top-level design. The top-level design is divided into a plurality of sub-modules. Each of the sub-modules is independently synthesized using RTL based design and independently conform to the timing requirements for the sub-modules produced through time-budgeting based on the top-level thing requirements. Once the sub-modules are synthesized and pass individual timing requirements specific for those sub-modules, the sub-modules are integrated to form a top-level design. The top-level design may then be verified for timing requirements and other formal requirements.

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